Design and Operation of Charge-Scaling DACs

Charge-scaling DAC is a popular DAC because of its low power dissipation, high speed, and good accuracy. The major disadvantage of charge-scaling DACs is large layout area for high resolution.

1. *Charge-Scaling Basics*

Consider the simple circuit shown in Fig. 1(a). The switch connects C_1 to ground initially and assume no charge store on C_1 and C_2. So v_{OUT} is zero. When C_1 is connected to V_{REF} via the switch as shown in Fig. 1(b), a current I flows through C_1 and C_2. The charge transferred to C_1 and C_2 are $\Delta Q_1 (=(V_{REF}-v_{OUT})\cdot C_1-0)$ and $\Delta Q_2 (=v_{OUT}\cdot C_2-0)$, respectively. Since C_1 and C_2 are in series, the same amount of charges are transferred to them, or $\Delta Q_1=\Delta Q_2$. Thus

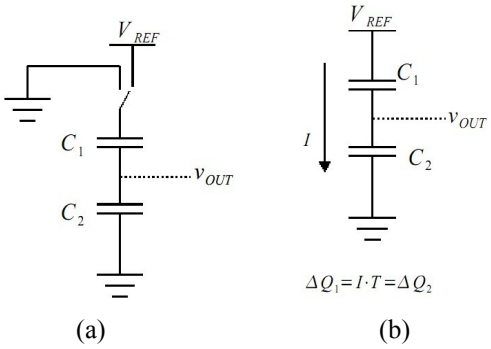


Figure 1: (a) Two capacitors in series, (b) the switch is connected to V_{REF}

$$v_{OUT}=\frac{C_1}{C_1+C_2}\cdot V_{REF}$$

The two capacitors work as a voltage divider. If C_1 can be changed while keeping (C_1+C_2) constant, a scaled output voltage can be obtained. This is the basic idea that charge-scaling DACs based on.

2. *Operation*

A basic N-bit charge-scaling DAC is shown in Fig. 2. The capacitor array consists of N+1 binary-weighted capacitors. The op-amp is in voltage follower configuration. The switches tied to the capacitors are control by the digital inputs $D_0, D_1, D_2, \ldots, D_N-1$. When the digital inputs are high, the corresponding capacitors are switched to V_{REF}, otherwise the capacitors are tied to ground.

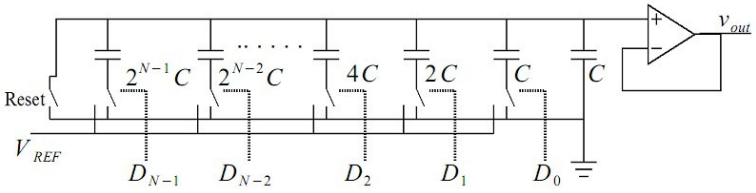


Figure 2: A N-bit charge-scaling DAC.

The sum of all capacitors is $2^N C$. The equivalent circuit with only the k-th digital input, D_k, is high, and other bits are set to zero is shown in Fig. 3. If there are other bits that are also high,

the output can be found by using superposition:

$$v_{OUT}=\sum_{k=0}^{N-1} D_k \cdot v_{OUT,k}=\sum_{k=0}^{N-1} D_k \cdot 2^{k-N} \cdot V_{REF}$$

See SPICE simulation ***Sim_1.asc*** for the operation of a basic charge-scaling DAC.

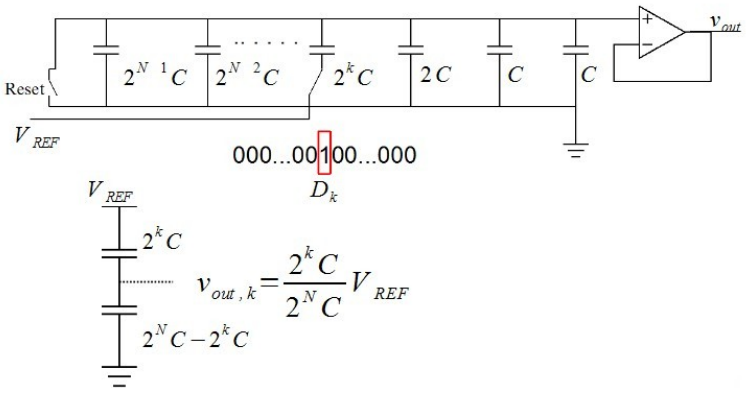


Figure 3: The equivalent circuit with $D_k=1$, and other bits are zero.

3. *Calculate INL/DNL*

The ratio of the capacitor array is critical for the charge-scaling DAC. Capacitor mismatch can cause large INL and DNL errors. The error in the ratio of the capacitor can be caused by undercutting of the mask and nonuniform oxide growth (Fig. 4). The solution to these problem is using unit capacitor and common-centroid scheme [2]. To calculate INL/DNL, assume the largest error of a unit capacitor is $|\Delta C_{max}|$, so the error of the k-th capacitor is $2^k \cdot |\Delta C_{max}|$. For example, the error of the MSB capacitor of a 4-bit DAC is $8|\Delta C_{max}|$. Further assume that the MSB capacitor is the only capacitor with a positive error (the errors of the other capacitors are all negative or zero), and sum of all the errors equals zero (Fig. 5).

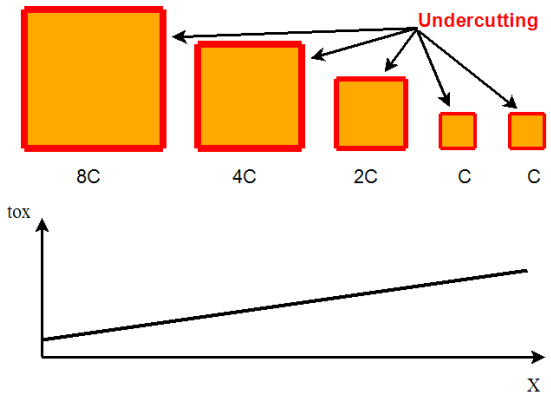


Figure 4: Capacitor mismatch of a 4-bit DAC

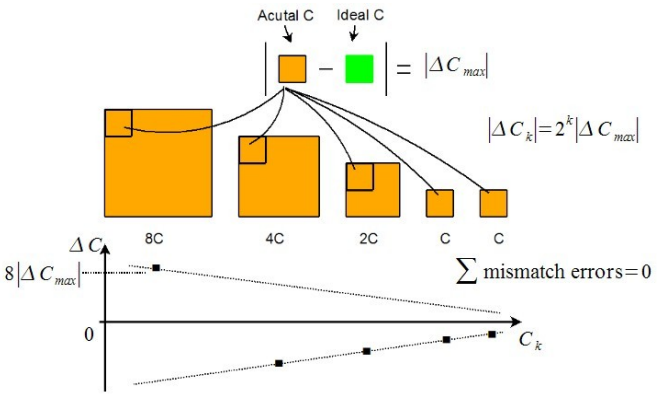


Figure 5: Estimate capacitor error

1) INL

After the capacitor error is introduced, the k-th output is

$$v_{OUT,k}=\frac{2^k C}{2^N C}V_{REF}\pm\frac{2^k}{2^N C}V_{REF}\frac{|\Delta C_{max}|}{C}$$

The first term is the ideal output, and the second term is the error due to the capacitor mismatch. Moving the first term to the left side results in the INL of the k-th output:

$$|INL|_k=2^k\frac{|\Delta C_{max}|}{C}LSB$$

The largest INL occurs when only the MSB capacitor is tied to V_{REF}, and the other capacitors are tied to ground:

$$|INL|_{max}=2^{N-1}\frac{|\Delta C_{max}|}{C}LSB$$

For INL to be within $1/2\,LSB$, the requirement for the mismatch is

$$\frac{|\Delta C_{max}|}{C}\leqslant\frac{1}{2^N}$$

The quantization error of a ideal 6-bit charge-scaling DAC shown in simulation ***Sim_2.asc*** illustrates the INL of the DAC. Simulation ***Sim_3.asc*** shows the quantization error of a 6-bit DAC with $|\Delta C_{max}|=1.56\,fF$.

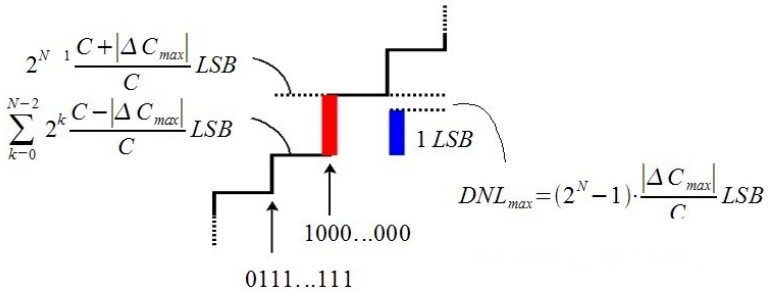


Figure 6: Maximum DNL

2) DNL

The worst-case DNL occurs when the digital code transitions from 0111...111 to 1000...000. As shown in Fig. 6, at the midpoint:

$$v_{OUT,1000...000}=2^{N-1}\frac{C+|\Delta C_{max}|}{C}LSB\ \text{ and }\ v_{OUT,0111...111}\sum_{k=0}^{N-2}2^k\frac{C-|\Delta C_{max}|}{C}LSB$$

The maximum DNL is difference of actual increment hight and the ideal increment high at the midpoint, or

$$DNL_{max}=v_{OUT,1000...000}-v_{OUT,0111...111}-1\,LSB=(2^N-1)\cdot\frac{|\Delta C_{max}|}{C}LSB$$

4. *The Split Array*

High resolution charge-scaling DAC requires large capacitors. For example, the largest capacitor (the MSB capacitor) required by a 12-bit DAC with unit capacitors equal 100 fF is $٢٠٤.٨\ pF\ (=٢^{١١}\cdot١٠٠\ fF)$. If this capacitor is fabricated using AMI's C5 process [3], its layout area is approximately $٤٧٧\times٤٧٧\ \mu m^{٢}$! To reduce the sizes of the capacitors, the split array is used. Fig. 7 shows a 6-bit DAC employing split array.

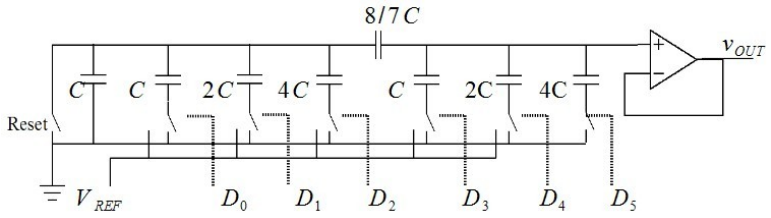


Figure 7: A 6-bit DAC with split array

The $٨/٧\,C$ capacitor is referred to attenuation capacitor. It is value can be found by

$$C_{atten}=\frac{\sum LSB\ array\ capacitors}{\sum MSB\ array\ capacitors}=\frac{C+C+٢C+٤C}{C+٢C+٤C}=\frac{٨}{٧}C$$

On each side of the attenuation capacitor is a 3-bit sub DAC. To understand this circuit, Thevenin theorem can be used as shown in Fig. 8.

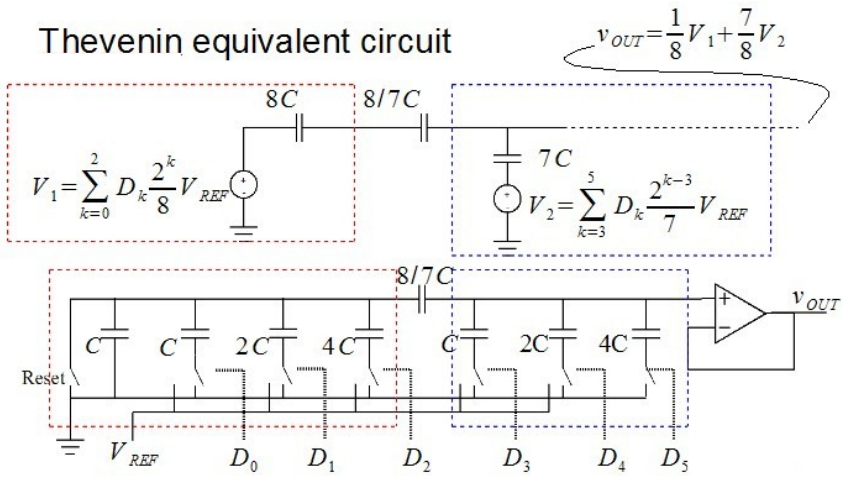


Figure 8: Thevenin equivalent circuit of the DAC with split array

Two sub DACs can be simplified to two Thevenin equivalent networks with two Thevenin equivalent voltage sources. The output can be found using superposition. The MSB capacitor in the split array is 400 fF (compared to the 3.2 pF MSB capacitor in the basic capacitor array). The operation of a 6-bit charge-scaling DAC with split array is shown in ***Sim_4.asc***.

5. *Issue and Other Topologies*

1) Parasitic Capacitance

The parasitic capacitance from the bottom plates of the capacitors to the substrate and the parasitic capacitance of the op-amp can cause error in the output. C_p in Fig. 9 models these capacitance. ***Sim_5.asc*** shows the quantization error of a 6-bit DAC with the parasitic capacitance equals ٥٠ fF .

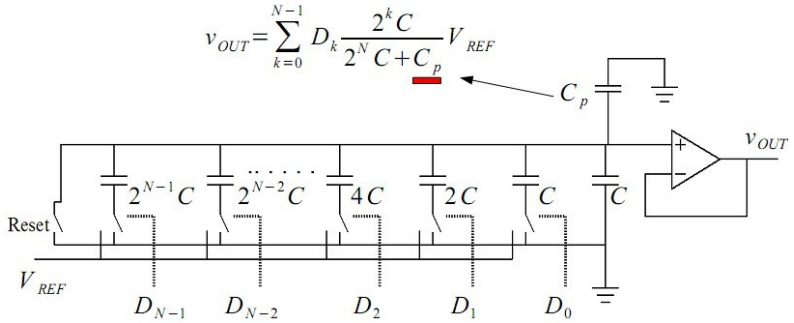


Figure 9: Parasitic capacitance in a charge-scaling DAC

To overcome this problem, the topology shown in Fig. 10 is used. The op-amp is no longer in voltage follower configuration and its plus input is connected to ground. Thus its minus input terminal, or the bottom plates of the capacitors, are at virtual ground. Since both terminals of C_p are grounded, it does not affect the circuit. When a capacitor is switched to V_{REF} , a current flows through it and C_F to the output. So the total output is

$$v_{OUT}=\sum_{k=٠}^{N-١} D_k \frac{٢^k C}{C_F} V_{REF}$$

Comparing the equation above with the one from the basic topology, we need to set $C_F=٢^N C$. This a much larger capacitor than the MSB capacitor. Thus the trade-off has to be made between accuracy and area. ***Sim_6.asc*** shows that the parasitic capacitance does not affect the output by using this topology.

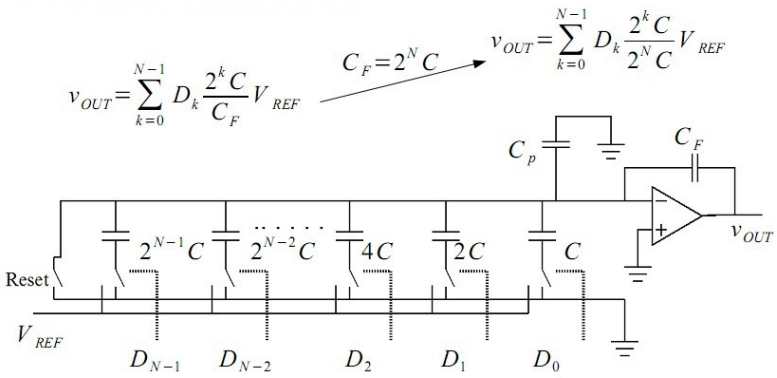


Figure 10: A different configuration of the op-amp

2) Op-amp Offset

Although the topology above can overcome the problem of parasitic capacitance, it is sensitive to the op-amp's offset. To compensate the offset, the topology in Fig. 11 can be used.

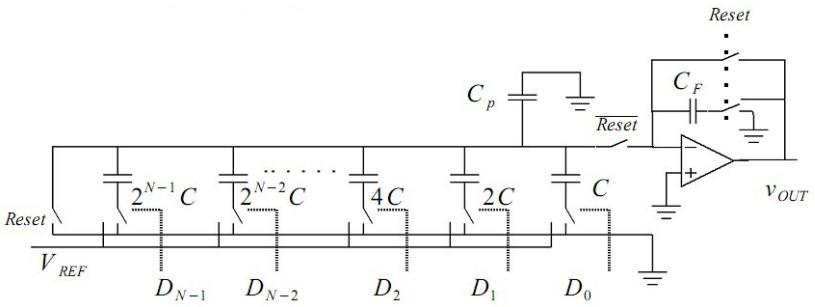
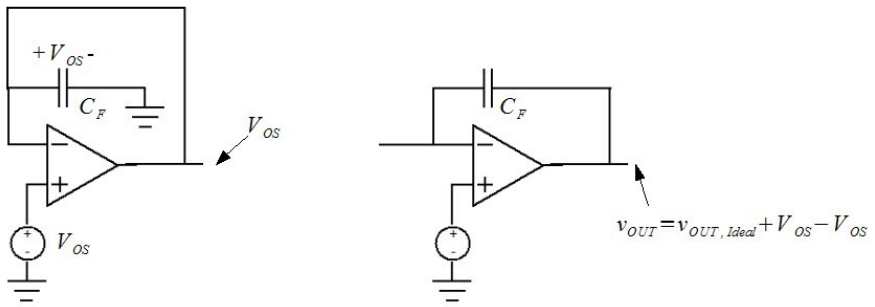


Figure 11: Topology for offset compensation

During the reset phase, the op-amp is disconnected from the capacitor array via $\overline{Reset}$ switch. The op-amp is in voltage follower configuration. The output equals V_{OS} . C_F is switched to ground thus the voltage across it is V_{OS} . After reset, the op-amp is connected to the capacitor array and the C_F is switched to the output node. The configuration during the normal operation mode is the same as the circuit shown in Fig. 10. The offset is cancel by the charge stored in C_F , and thus the output is not affected by the offset. Fig. 12 illustrates this concept.



(a) Reset mode (b) Normal mode

Figure 12: Offset compensation

6. Summary

Charge-scaling DACs require large layout area for high resolution. To make the DAC insensitive to the parasitic capacitance, an even larger capacitor may be required. The advantages of the charge-scaling DAC is low power dissipation (the capacitor array does not dissipate static power), high speed, and the offset can be compensated easily using switch-capacitor circuit.

Reference

[1] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*, 2nd ed, Wiley-IEEE, 2005.

[2] J. L. McCreary and P. R. Gray, *All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques*, Part I, IEEE Journal of Solid State Circuits, vol. 10, no. 6, pp. 371-379, Dec. 1975.

[3] http://www.mosis.com/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t68z-params.txt

[4] http://www.aicdesign.org/SCNOTES/2006notes/Chap10(12_8_06).pdf